

In The Claims

Applicant submits below a complete listing of the current claims, with any insertions indicated by underlining and any deletions indicated by strikeouts and/or double bracketing.

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of the Claims

1. (Currently amended) A capacitor having a first electrode formed of a heavily-doped active region (~~D~~) of a semiconductor component (~~T~~) formed on the side of a surface of a semiconductor bulk, characterized in that the second electrode formed of a conductive region (~~BR~~) coated with an insulator (~~IL~~) formed under said active region and embedded in the semiconductor bulk.

2. (Currently amended) The capacitor of claim 1, wherein the coated conductive region comprises an extension above a portion of which is formed a contact opening (~~V~~) towards the second electrode.

3. (Currently amended) The capacitor of claim 2, wherein the heavily-doped active region is the drain (~~D~~) or source region of a MOS transistor (~~T~~).

4. (Currently amended) An SRAM cell comprising two inverters (~~I1, I2~~) head-to-tail, each of which comprises two MOS transistors of two conductivity types (~~TN1, TP1; TN2, TP2~~) formed side by side, having their drains connected to each other and having their gates connected to each other, and comprising two capacitors (~~C1, C2~~) of claim 3, the respective first electrodes of which are the drains (~~D~~) of said transistors and the second electrodes of which are a same coated region (~~BR1, BR2~~) connected to the gates (~~G~~) of said transistors via a contact opening (~~V1, V2~~) formed between the two transistors.

5. (Currently amended) A DRAM cell comprising a MOS transistor (~~TC~~) having its source region (~~S~~) connected to a bit line, having its gate (~~G~~) connected to a word line, and

comprising a capacitor (C) of claim 3, the first electrode of which is the drain region (D) of said transistor and the second electrode of which is a coated region (BR) connected to a supply line.

6. (Currently amended) An integrated circuit comprising a capacitor according to ~~any of claims 1 to 3~~ claim 1 ~~comprising a memory cell according to claim 4 or 5~~, wherein the insulator (IL1) coating the lower surface of the coated region (BR1) exhibits a ~~stronger~~ larger dielectric constant than the insulator (IL2) coating the rest of the coated conductive region.

7. (Currently amended) A method for manufacturing a capacitor having a first electrode formed of a heavily-doped active region (D) of a semiconductor component, ~~comprising the steps of:~~

a/ forming at the surface of an initial semiconductor substrate (SUB) a conductive region (BR1) coated with an insulator;

b/ growing by epitaxy a semiconductor layer (10) to cover the initial substrate and bury the coated region (BR1);

c/ forming said heavily-doped active region (D) across the entire thickness of said semiconductor layer (10), above a portion of the coated conductive region (BR1).

8. (Currently amended) The method of claim 7, wherein the heavily-doped active region is one of the drain region (D) and of the source region of a MOS transistor (TP1, TN1).

9. (Currently amended) The method of claim 8, wherein, before forming the drain and source regions, an opening (V1) is made above another portion of the coated conductive region (BR1) in said semiconductor layer (10) and in the insulator (IL2) coating the conductive region (BR1) to connect the conductive region (BR1) to a conductive layer used to form the gate (G) of the transistor (TP1, TN1).

10. (Currently amended) The method of claim 9, wherein the opening (V1) is made at the step of digging the STI insulation trenches of said MOS transistor.